Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (Cancelled)

Claim 6 (Previously Presented): A high density ROM cell installed on a silicon substrate for storing data, comprising:

a plurality of drain doped regions being of a second conductive type installed on the silicon substrate;

a source doped region being of the second conductive type installed on the silicon substrate; and

a gate installed on the surface of the silicon substrate and adjacent to the plurality of drain doped regions and the source doped region, the gate having at least one extension structure respectively located between one of the plurality of drain doped regions and another drain doped region so that a plurality of drain signals respectively passing through the plurality of drain doped regions do not interfere with each other.

Claim 7 (Previously Presented): The ROM cell of claim 6 installed in a doped well being of a first conductive type on the silicon substrate.

Claim 8 (Original): The ROM cell of claim 7 wherein the first conductive type is P-type, and the second conductive type is N-type.

Claim 9 (Original): The ROM cell of claim 7 wherein the first conductive type is N-type, and the second conductive type is P-type.

Claim 10 (Original): The ROM cell of claim 6 wherein the second conductive type is N-type.

Claim 11 (Original): The ROM cell of claim 6 wherein the second conductive type is P-type.

Claim 12 (Cancelled)

Claim 13 (Previously Presented): A read-only memory (ROM) memory array installed on a silicon substrate, the memory array comprising a plurality of high density ROM cells, each ROM cell comprising:

a common gate installed on the surface of the silicon substrate;

a common source of a first conductive type installed on the silicon substrate adjacent to the common gate; and

a plurality of heavily doped drains of a second conductive type installed within a doped region of the first conductive type on the silicon substrate, the doped region of the first conductive type being adjacent to the common gate.

Claim 14 (Previously Presented): The memory array of claim 13 further comprising a plurality of bit lines connected to the plurality of ROM cells installed on the silicon substrate.

Claim 15 (Previously Presented): The memory array of claim 14 wherein a number of bit lines connected to one of the plurality of ROM cells is equal to the number of heavily doped drains for said one of the plurality of ROM cells.

Claim 16 (Previously Presented): The memory array of claim 15 wherein each of the heavily doped drains for said one of the plurality of ROM cells is connected to a different bit line.

Claim 17 (Previously Presented): The memory array of claim 16 further comprising a switch connected to the plurality of bit lines for selectively accessing one of the heavily doped drains of said one of the plurality of ROM cells.

Claim 18 (Previously Presented): The memory array of claim 13 further comprising means of individually storing data or accessing data stored in each of the heavily doped drains of one of the plurality of ROM cells utilizing the common gate and the common source of said one of the plurality of ROM cells.